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Jameco Part Number 173534

HEWLETT PACKARD

AC/DC to Logic Interface Optocouplers

Technical Data

HCPL-3700
HCPL-3760

Features

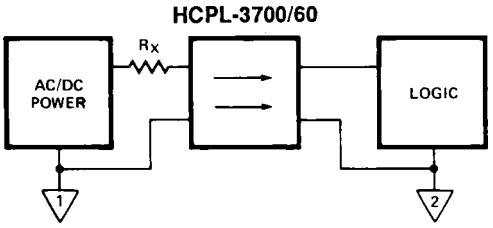
- **Standard (HCPL-3700) and Low Input Current (HCPL-3760) Versions**
- **AC or DC Input**
- **Programmable Sense Voltage**
- **Hysteresis**
- **Logic Compatible Output**
- **Thresholds Guaranteed over Temperature**
- **Thresholds Independent of LED Optical Parameters**
- **Recognized under UL 1577 and CSA Approved for Dielectric Withstand Proof Test Voltage of 2500 Vac, 1 Minute**

Applications

- **Limit Switch Sensing**
- **Low Voltage Detector**
- **5 V-240 V AC/DC Voltage Sensing**
- **Relay Contact Monitor**
- **Relay Coil Voltage Monitor**
- **Current Sensing**
- **Microprocessor Interfacing**

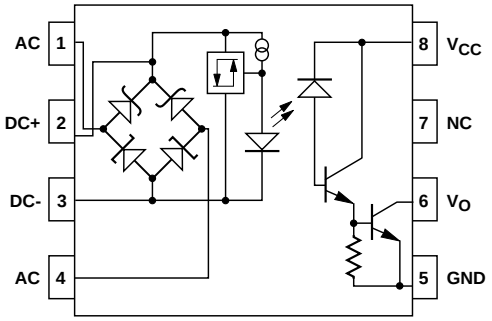
Description

The HCPL-3700 and HCPL-3760 are voltage/current threshold detection optocouplers. The HCPL-3760 is a low-current version of the HCPL-3700. To obtain lower current operation, the HCPL-3760 uses a high-efficiency AlGaAs LED which provides higher light output at lower drive currents. Both devices utilize threshold sensing input buffer ICs which permit control of threshold levels over a wide range of input voltages with a single external resistor.



The input buffer incorporates several features: hysteresis for extra noise immunity and switching immunity, a diode bridge for easy use with ac input signals, and internal clamping

Functional Diagram



TRUTH TABLE (POSITIVE LOGIC)

INPUT	OUTPUT
H	L
L	H

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

diodes to protect the buffer and LED from a wide range of over-voltage and over-current transients. Because threshold sensing is done prior to driving the LED, variations in optical coupling from the LED to the detector will have no effect on the threshold levels.

The HCPL-3700's input buffer IC has a nominal turn on threshold of 2.5 mA (I_{TH} +) and 3.7 volts (V_{TH} +).

The buffer IC for the HCPL-3760 was redesigned to permit a lower input current. The nominal turn on threshold for the HCPL-3760 is 1.2 mA (I_{TH} +) and 3.7 volts (V_{TH} +).

The high gain output stage features an open collector output providing both TTL compatible saturation voltages and CMOS compatible breakdown voltages.

By combining several unique functions in a single package, the user is provided with an ideal component for industrial control computer input boards and other applications where a predetermined input threshold level is desirable.

Ordering Information

Specify Part Number followed by Option Number (if desired)

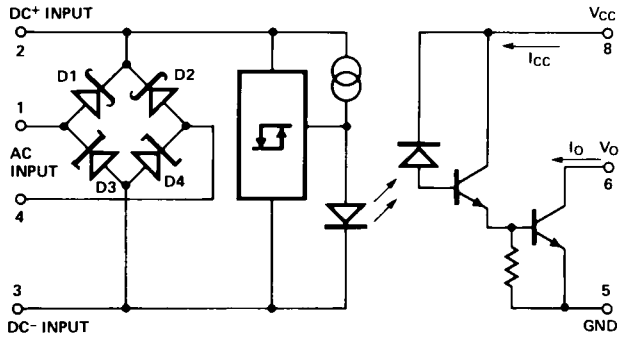
Example

HCPL-3700#XXX

- 300 = Gull Wing Surface Mount Option
- 500 = Tape/Reel Package Option (1 K min.)

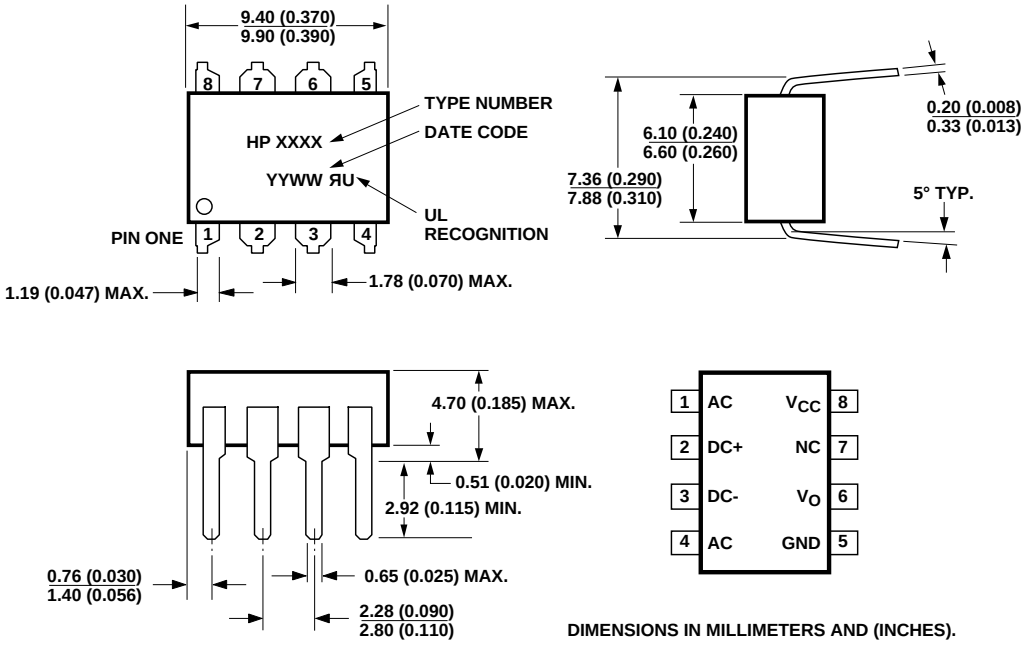
Option data sheets available. Contact your Hewlett-Packard sales representative or authorized distributor for information.

Schematic



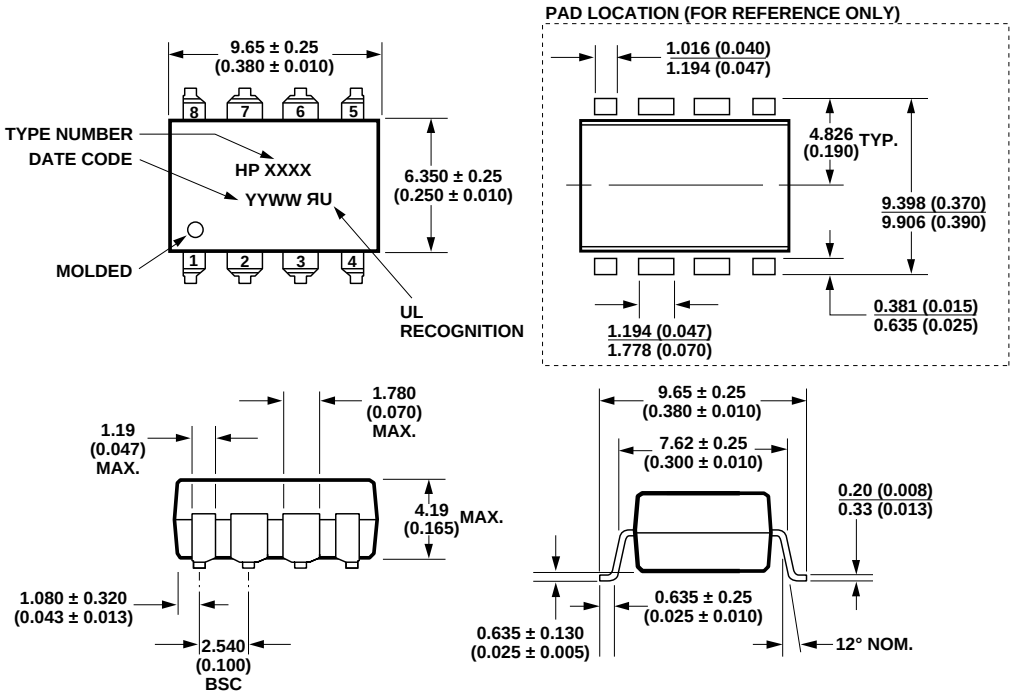
Package Outline Drawings

Standard DIP Package



DIMENSIONS IN MILLIMETERS AND (INCHES).

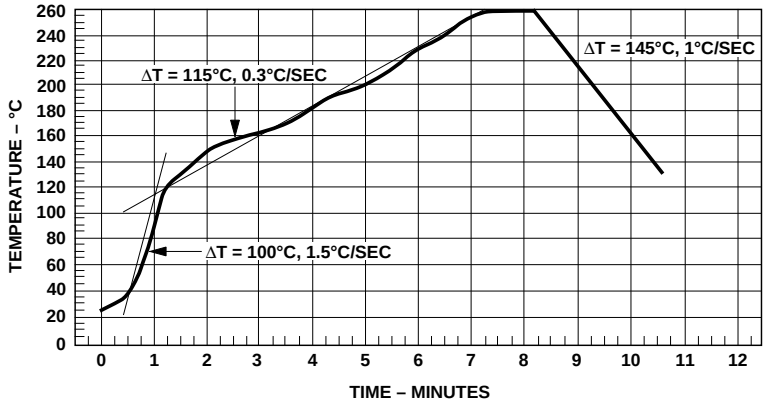
Gull Wing Surface Mount Option 300



DIMENSIONS IN MILLIMETERS (INCHES).
TOLERANCES (UNLESS OTHERWISE SPECIFIED): xx.xx = 0.01
xx.xxx = 0.005

LEAD COPLANARITY
MAXIMUM: 0.102 (0.004)

Maximum Solder Reflow Thermal Profile



(NOTE: USE OF NON-CHLORINE ACTIVATED FLUXES IS RECOMMENDED.)

Regulatory Information

The HCPL-3700/60 has been approved by the following organizations:

UL

Recognized under UL 1577, component recognition program, File E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (External Clearance)	L(IO1)	7.1	mm	Measured from input terminals to output terminals, shortest distance through air
Min. External Tracking Path (External Creepage)	L(IO2)	7.4	mm	Measured from input terminals to output terminals, shortest distance path along body
Min. Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity
Tracking Resistance (Comparative Tracking Index)	CTI	200	V	DIN IEC 112/VDE 0303 PART 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 – surface mount classification is Class A in accordance with CECC 00802.

Absolute Maximum Ratings (No derating required up to 70°C)

Parameter		Symbol	Min.	Max.	Units	Note
Storage Temperature		T_S	-55	125	°C	
Operating Temperature		T_A	-40	85	°C	
Lead Soldering Cycle	Temperature			260	°C	1
	Time			10	s	
Input Current	Average	I_{IN}		50	mA	2
	Surge			140		2, 3
	Transient			500		
Input Voltage (Pins 2-3)		V_{IN}	-0.5		V	
Input Power Dissipation		P_{IN}		230	mW	4
Total Package Power Dissipation		P_T		305	mW	5
Output Power Dissipation		P_O		210	mW	6
Output Current	Average	I_O		30	mA	7
Supply Voltage (Pins 8-5)		V_{CC}	-0.5	20	V	
Output Voltage (Pins 6-5)		V_O	-0.5	20	V	
Solder Reflow Temperature Profile		See Package Outline Drawings section				

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
Supply Voltage	V_{CC}	2	18	V	
Operating Temperature	T_A	0	70	°C	
Operating Frequency	f	0	4	kHz	8

Electrical Specifications

Over Recommended Temperature T_A = 0°C to 70°C, Unless Otherwise Specified.

Parameter		Sym.	Device	Min.	Typ.[9]	Max.	Units	Conditions	Fig.	Note
Input Threshold Current		I_{TH+}	HCPL-3700	1.96	2.5	3.11	mA	$V_{IN} = V_{TH+}$; V_{CC} = 4.5 V; V_O = 0.4 V; $I_O \geq$ 4.2 mA	2, 3	14
			HCPL-3760	0.87	1.2	1.56				
		I_{TH-}	HCPL-3700	1.00	1.3	1.62		$V_{IN} = V_{TH-}$; V_{CC} = 4.5 V; V_O = 2.4 V; $I_{OH} \leq$ 100 µA		
			HCPL-3760	0.43	0.6	0.80				
Input Threshold Voltage	DC (Pins 2, 3)	V_{TH+}		3.35	3.7	4.05	V	$V_{IN} = V_2 - V_3$; Pins 1 & 4 Open V_{CC} = 4.5 V; V_O = 0.4 V; $I_O \geq$ 4.2 mA		
		V_{TH-}		2.01	2.6	2.86	V	$V_{IN} = V_2 - V_3$; Pins 1 & 4 Open V_{CC} = 4.5 V; V_O = 2.4 V; $I_O \leq$ 100 µA		
	AC (Pins 1, 4)	V_{TH+}		4.23	4.9	5.50	V	$V_{IN} = \lvert V_1 - V_4 \rvert$; Pins 2 & 3 Open V_{CC} = 4.5 V; V_O = 0.4 V; $I_O \geq$ 4.2 mA		14, 15
		V_{TH-}		2.87	3.7	4.20	V	$V_{IN} = \lvert V_1 - V_4 \rvert$; Pins 2 & 3 Open V_{CC} = 4.5 V; V_O = 2.4 V; $I_O \leq$ 100 µA		
Hysteresis		I_{HYS}	HCPL-3700		1.2		mA	$I_{HYS} = I_{TH+} - I_{TH-}$	2	
			HCPL-3760		0.6					
		V_{HYS}			1.2		V	$V_{HYS} = V_{TH+} - V_{TH-}$		
Input Clamp Voltage		V_{IHC1}		5.4	6.0	6.6	V	$V_{IHC1} = V_2 - V_3$; V_3 = GND; I_{IN} = 10 mA; Pins 1 & 4 Connected to Pin 3	1	
		V_{IHC2}		6.1	6.7	7.3	V	$V_{IHC2} = \lvert V_1 - V_4 \rvert$; $\lvert I_{IN} \rvert$ = 10 mA; Pins 2 & 3 Open		
		V_{IHC3}			12.0	13.4	V	$V_{IHC3} = V_2 - V_3$; V_3 = GND; I_{IN} = 15 mA; Pins 1 & 4 Open		
		V_{ILC}			-0.76		V	$V_{ILC} = V_2 - V_3$; V_3 = GND; I_{IN} = -10 mA		
Input Current		I_{IN}	HCPL-3700	3.0	3.7	4.4	mA	$V_{IN} = V_2 - V_3$ = 5.0 V Pins 1 & 4 Open	5	
			HCPL-3760	1.5	1.8	2.2				
Bridge Diode Forward Voltage		$V_{D1,2}$	HCPL-3700		0.59		V	I_{IN} = 3 mA		
			HCPL-3760		0.51			I_{IN} = 1.5 mA		
		$V_{D3,4}$	HCPL-3700		0.74			I_{IN} = 3 mA		
			HCPL-3760		0.71			I_{IN} = 1.5 mA		
Logic Low Output Voltage		V_{OL}			0.1	0.4	V	V_{CC} = 4.5 V; I_{OL} = 4.2 mA	5	14
Logic High Output Current		I_{OH}				100	µA	$V_{OH} = V_{CC}$ = 18 V		14
Logic Low Supply Current		I_{CCL}	HCPL-3700		1.2	4	mA	$V_2 - V_3$ = 5.0 V; V_O = Open; V_{CC} = 5.0 V	6	
			HCPL-3760		0.7	3				
Logic High Supply Current		I_{CCH}			0.002	4	µA	V_{CC} = 18 V; V_O = Open	4	14
Input Capacitance		C_{IN}			50		pF	f = 1 MHz; V_{IN} = 0 V, Pins 2 & 3, Pins 1 & 4 Open		

Switching Specifications

T_A = 25°C, V_{CC} = 5.0 V, Unless Otherwise Specified.

Parameter	Sym.	Device	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}	HCPL-3700		4.0	15.0	µs	R_L = 4.7 kΩ, C_L = 30 pF	7, 10	10
		HCPL-3760		4.5					
Propagation Delay Time to Logic High at Output	t_{PLH}	HCPL-3700		10.0	40.0	µs	R_L = 4.7 kΩ, C_L = 30 pF		11
		HCPL-3760		8.0					
Output Rise Time (10-90%)	t_r	HCPL-3700		20		µs	R_L = 4.7 kΩ, C_L = 30 pF	8	
		HCPL-3760		14					
Output Fall Time (90-10%)	t_f	HCPL-3700		0.3		µs	R_L = 4.7 kΩ, C_L = 30 pF		
		HCPL-3760		0.4					
Common Mode Transient Immunity at Logic High Output	$\|CM_H\|$			4000		V/µs	I_{IN} = 0 mA, R_L = 4.7 kΩ, $V_{O\ min}$ = 2.0 V, V_{CM} = 1400 V	9, 11	12, 13
Common Mode Transient Immunity at Logic Low Output	$\|CM_L\|$	HCPL-3700		600		V/µs	I_{IN} = 3.11 mA; R_L = 4.7 kΩ, $V_{O\ max}$ = 0.8 V, V_{CM} = 140 V		
		HCPL-3760					I_{IN} = 1.56 mA; R_L = 4.7 kΩ, $V_{O\ max}$ = 0.8 V, V_{CM} = 140 V		

Package Characteristics

Over Recommended Temperature T_A = 0°C to 70°C, Unless Otherwise Specified.

Parameter	Sym.	Min.	Typ.[9]	Max.	Units	Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage*	V_{ISO}	2500			V rms	RH ≤ 50%, t = 1 min; T_A = 25°C		16, 17
Input-Output Resistance	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 Vdc		16
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1 MHz; V_{I-O} = 0 Vdc		

*The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Characteristics Table (if applicable), your equipment level safety specification, or HP Application Note 1074, "Optocoupler Input-Output Endurance Voltage."

Notes:

1. Measured at a point 1.6 mm below seating plane.
2. Current into/out of any single lead.
3. Surge input current duration is 3 ms at 120 Hz pulse repetition rate. Transient input current duration is 10 μs at 120 Hz pulse repetition rate. Note that maximum input power, P_{IN}, must be observed.
4. Derate linearly above 70°C free-air temperature at a rate of 4.1 mW/°C. Maximum input power dissipation of 230 mW allows an input IC junction temperature of 125°C at an ambient temperature of T_A = 70°C with a typical thermal resistance from junction to ambient of θ_{JA1} = 240°C/W. Excessive P_{IN} and T_J may result in IC chip degradation.
5. Derate linearly above 70°C free-air temperature at a rate of 5.4 mW/°C.
6. Derate linearly above 70°C free-air temperature at a rate of 3.9 mW/°C. Maximum output power dissipation of 210 mW allows an output IC junction temperature of 125°C at an ambient temperature of T_A = 70°C with a typical thermal resistance from junction to ambient of θ_{JA0} = 265°C/W.
7. Derate linearly above 70°C free-air temperature at a rate of 0.6 mA/°C.
8. Maximum operating frequency is defined when output waveform Pin 6 obtains only 90% of V_{CC} with R_L = 4.7 kΩ, C_L = 30 pF using a 5 V square wave input signal.
9. All typical values are at T_A = 25°C, V_{CC} = 5.0 V unless otherwise stated.
10. The t_{PHL} propagation delay is measured from the 2.5 V level of the leading edge of a 5.0 V input pulse (1 μs rise time) to the 1.5 V level on the leading edge of the output pulse (see Figure 10).
11. The t_{PLH} propagation delay is measured from the 2.5 V level of the trailing edge of a 5.0 V input pulse (1 μs fall time) to the 1.5 V level on the trailing edge of the output pulse (see Figure 10).
12. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to insure that the output will remain in a Logic High state (i.e., V_O > 2.0 V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to insure that the output will remain in a Logic Low state (i.e., V_O < 0.8 V). See Figure 11.
13. In applications where dV_{CM}/dt may exceed 50,000 V/μs (such as static discharge), a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value for R_{CC} is 240 Ω per volt of allowable drop in V_{CC} (between Pin 8 and V_{CC}) with a minimum value of 240 Ω.
14. Logic low output level at Pin 6 occurs under the conditions of $V_{IN} \geq V_{TH+}$ as well as the range of $V_{IN} > V_{TH-}$ once V_{IN} has exceeded V_{TH+}. Logic high output level at Pin 6 occurs under the conditions of $V_{IN} \leq V_{TH-}$ as well as the range of $V_{IN} < V_{TH+}$ once V_{IN} has decreased below V_{TH-}.
15. AC voltage is instantaneous voltage.
16. Device considered a two terminal device: Pins 1, 2, 3, 4 connected together, and Pins 5, 6, 7, 8 connected together.
17. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V rms for 1 second (leakage detection current limit, $I_{i-o} \leq$ 5 μA).

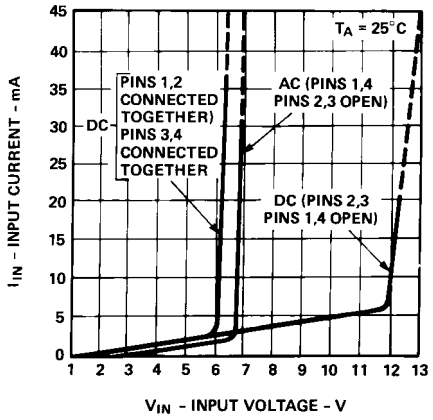
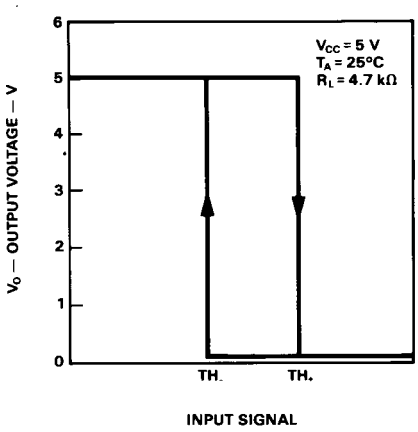


Figure 1. Typical Input Characteristics, I_{IN} vs. V_{IN} (AC Voltage is Instantaneous Value).



	DEVICE	TH_+	TH_-	INPUT CONNNECTION
I_{TH}	HCPL-3700	2.5 mA	1.3 mA	PINS 2, 3
	HCPL-3760	1.2 mA	0.6 mA	OR 1, 4
$V_{TH(dc)}$	BOTH	3.7 V	2.6 V	PINS 2, 3
$V_{TH(ac)}$	BOTH	4.9 V	3.7 V	PINS 1, 4

Figure 2. Typical Transfer Characteristics.

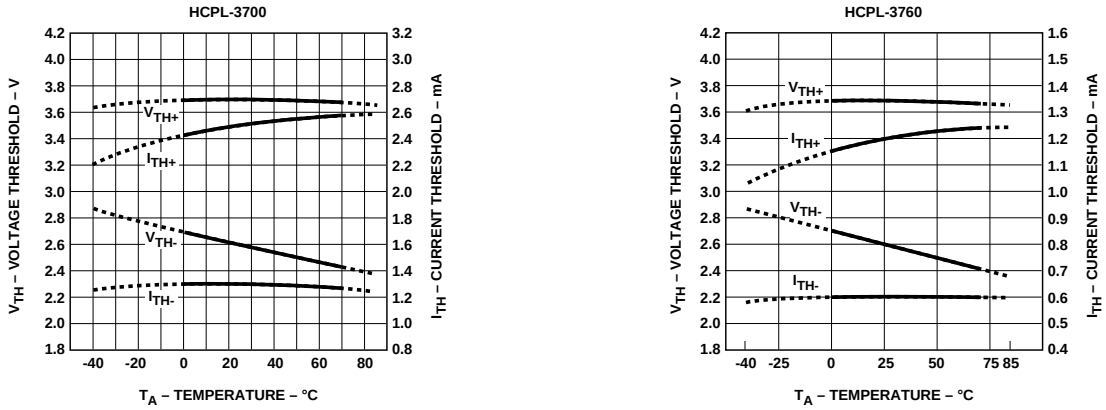


Figure 3. Typical DC Threshold Levels vs. Temperature.

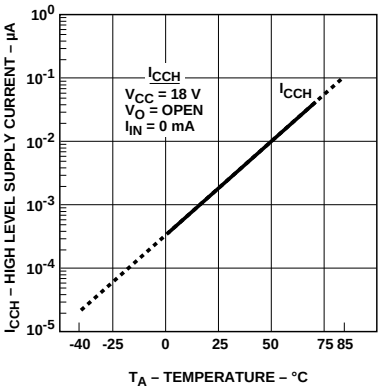


Figure 4. Typical High Level Supply Current, I_{CCH} vs. Temperature.

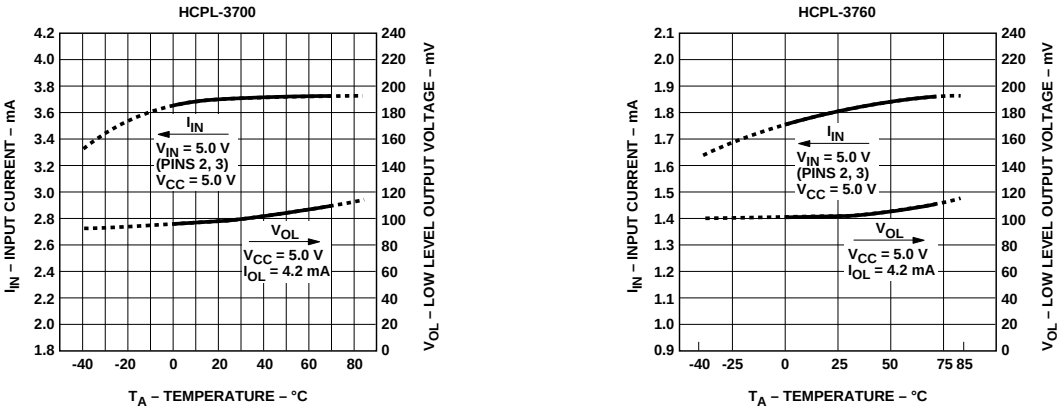

HCPL-3700
I_{IN} – INPUT CURRENT – mA
V_{OL} – LOW LEVEL OUTPUT VOLTAGE – mV
I_{IN}
V_{IN} = 5.0 V
(PINS 2, 3)
V_{CC} = 5.0 V
V_{OL}
V_{CC} = 5.0 V
I_{OL} = 4.2 mA
-40 -20 0 20 40 60 80
T_A – TEMPERATURE – °C
HCPL-3760
I_{IN} – INPUT CURRENT – mA
V_{OL} – LOW LEVEL OUTPUT VOLTAGE – mV
I_{IN}
V_{IN} = 5.0 V
(PINS 2, 3)
V_{CC} = 5.0 V
V_{OL}
V_{CC} = 5.0 V
I_{OL} = 4.2 mA
-40 -25 0 25 50 75 85
T_A – TEMPERATURE – °C

Figure 5. Typical Input Current, I_{IN}, and Low Level Output Voltage, V_{OL}, vs. Temperature.

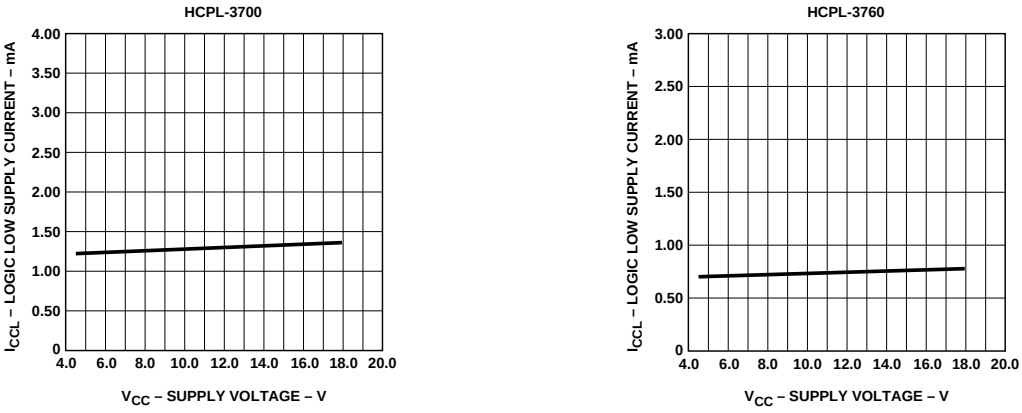


Figure 6. Typical Logic Low Supply Current vs. Supply Voltage.

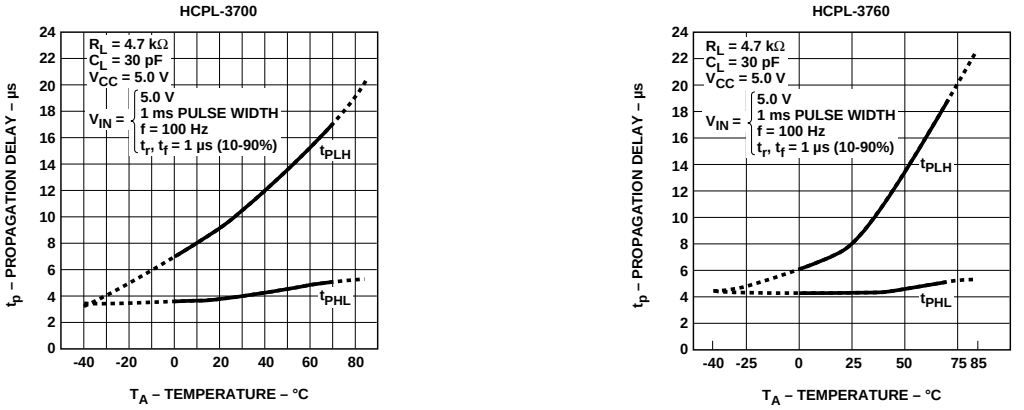

HCPL-3700
R_L = 4.7 kΩ
C_L = 30 pF
V_{CC} = 5.0 V
V_{IN} = 5.0 V, 1 ms PULSE WIDTH, f = 100 Hz, t_r, t_f = 1 µs (10-90%)
t_{PLH}
t_{PHL}
t_p – PROPAGATION DELAY – µs
T_A – TEMPERATURE – °C
HCPL-3760
R_L = 4.7 kΩ
C_L = 30 pF
V_{CC} = 5.0 V
V_{IN} = 5.0 V, 1 ms PULSE WIDTH, f = 100 Hz, t_r, t_f = 1 µs (10-90%)
t_{PLH}
t_{PHL}
t_p – PROPAGATION DELAY – µs
T_A – TEMPERATURE – °C

Figure 7. Typical Propagation Delay vs. Temperature.

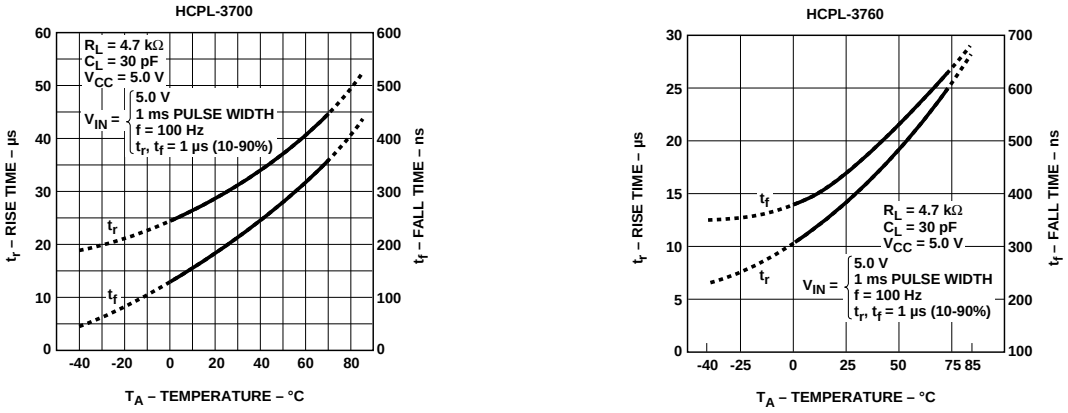

HCPL-3700
R_L = 4.7 kΩ
C_L = 30 pF
V_{CC} = 5.0 V
V_{IN} = 5.0 V, 1 ms PULSE WIDTH, f = 100 Hz, t_r, t_f = 1 µs (10-90%)
t_r
t_f
t_r – RISE TIME – µs
t_f – FALL TIME – ns
T_A – TEMPERATURE – °C
HCPL-3760
R_L = 4.7 kΩ
C_L = 30 pF
V_{CC} = 5.0 V
V_{IN} = 5.0 V, 1 ms PULSE WIDTH, f = 100 Hz, t_r, t_f = 1 µs (10-90%)
t_f
t_r
t_r – RISE TIME – µs
t_f – FALL TIME – ns
T_A – TEMPERATURE – °C

Figure 8. Typical Rise, Fall Times vs. Temperature.

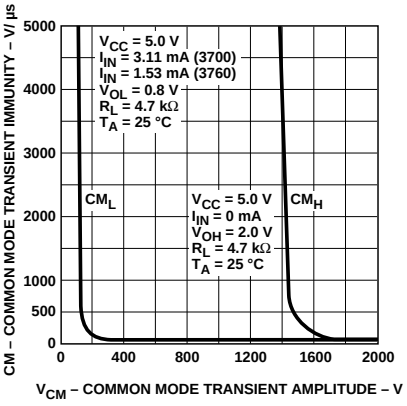

V_{CC} = 5.0 V
I_{IN} = 3.11 mA (3700)
I_{IN} = 1.53 mA (3760)
V_{OL} = 0.8 V
R_L = 4.7 kΩ
T_A = 25 °C
CM_L
V_{CC} = 5.0 V
I_{IN} = 0 mA
V_{OH} = 2.0 V
R_L = 4.7 kΩ
T_A = 25 °C
CM_H
CM – COMMON MODE TRANSIENT IMMUNITY – V/ µs
V_{CM} – COMMON MODE TRANSIENT AMPLITUDE – V

Figure 9. Common Mode Transient Immunity vs. Common Mode Transient Amplitude.

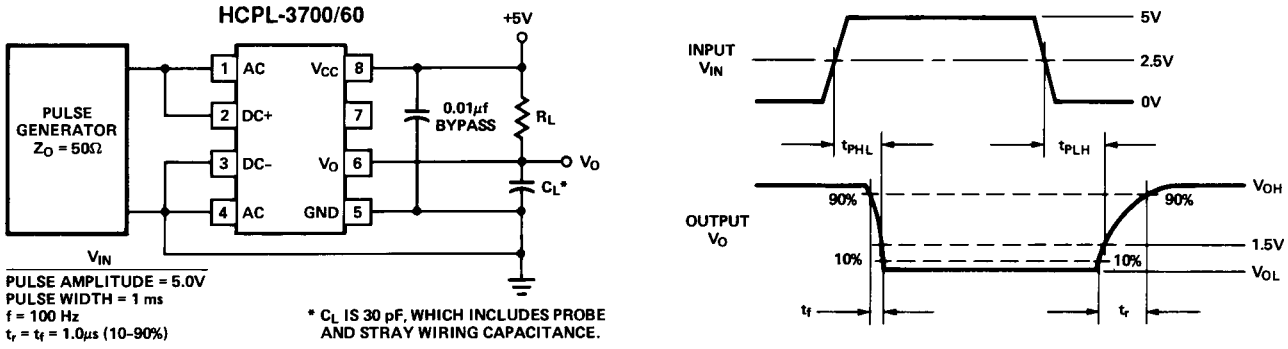


Figure 10. Switching Test Circuit.

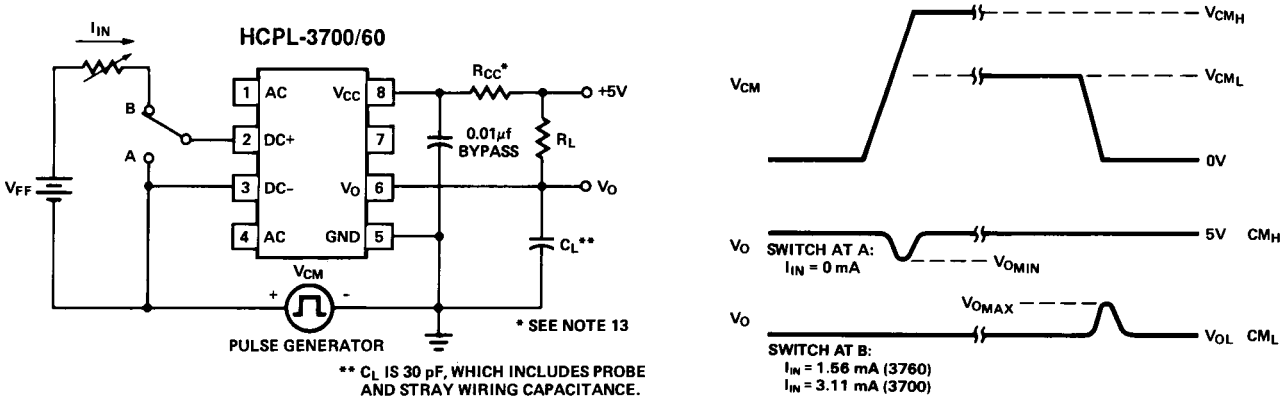


Figure 11. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

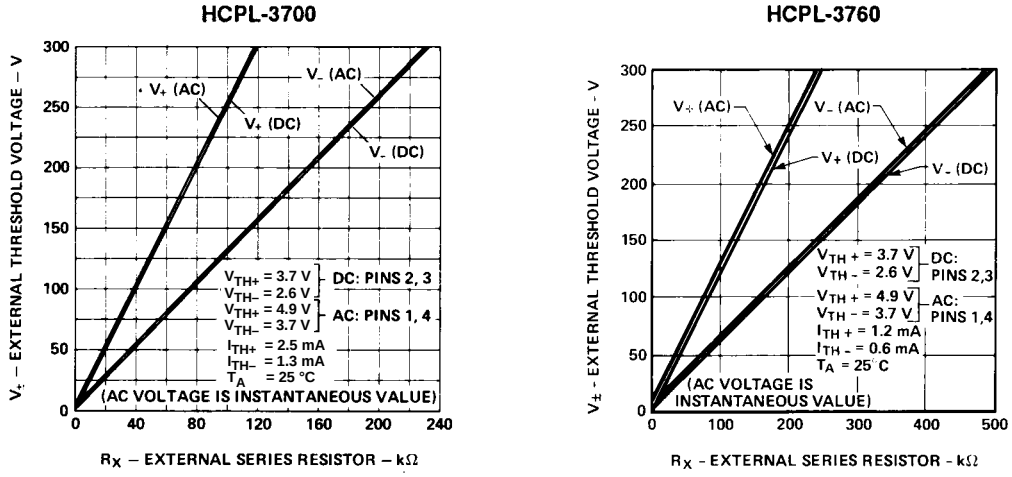


Figure 12. Typical External Threshold Characteristics, V± vs. R_X.

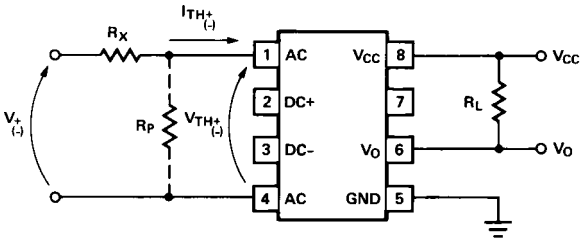


Figure 13. External Threshold Voltage Level Selection.

Electrical Considerations

The HCPL-3700/3760 optocouplers have internal temperature compensated, predictable voltage and current threshold points which allow selection of an external resistor, R_X, to determine larger external threshold voltage levels. For a desired external threshold voltage, $V_{\pm}$, a corresponding typical value of R_X can be obtained from Figure 12. Specific calculation of R_X can be obtained from Equation (1). Specification of both V_+ and V_- voltage threshold levels simultaneously can be obtained by the use of R_X and R_P as shown in Figure 13 and determined by Equations (2) and (3).

R_X can provide over-current transient protection by limiting input current during a transient condition. For monitoring contacts of a relay or switch, the HCPL-3700/3760 in combination with R_X and R_P can be used to allow a specific current to be conducted through the contacts for cleaning purposes (wetting current).

The choice of which input voltage clamp level to choose depends upon the application of this device (see Figure 1). It is recommended that the low clamp condition be used when possible.

The low clamp condition in conjunction with the low input current feature will ensure extremely low input power dissipation.

In applications where dV_{CM}/dt may be extremely large (such as static discharge), a series resistor, R_{CC}, should be connected in series with V_{CC} and Pin 8 to protect the detector IC from destructively high surge currents. See Note 13 for determination of R_{CC}. In addition, it is recommended that a ceramic disc bypass capacitor of 0.01 µF be placed between Pins 8 and 5 to reduce the effect of power supply noise.

For interfacing ac signals to TTL systems, output low pass filtering can be performed with a pullup resistor of 1.5 kΩ and 20 µF capacitor. This application requires a Schmitt trigger gate to avoid slow rise time chatter problems. For ac input applications, a filter capacitor can be placed across the dc input terminals for either signal or transient filtering.

Either ac (Pins 1, 4) or dc (Pins 2, 3) input can be used to determine external threshold levels.

For one specifically selected external threshold voltage level V_+ or V_-, R_X can be determined without use of R_P via

$$R_X = \frac{V_+ - V_{TH+}(-)}{I_{TH+}(-)} \quad (1)$$

For two specifically selected external threshold voltage levels, V_+ and V_-, the use of R_X and R_P will permit this selection via equations (2), (3) provided the following conditions are met. If the denominator of equation (2) is positive, then

$$\frac{V_+}{V_-} \geq \frac{V_{TH+}}{V_{TH-}} \text{ and } \frac{V_+ - V_{TH+}}{V_- - V_{TH-}} < \frac{I_{TH+}}{I_{TH-}}$$

Conversely, if the denominator of equation (2) is negative, then

$$\frac{V_+}{V_-} \leq \frac{V_{TH+}}{V_{TH-}} \text{ and } \frac{V_+ - V_{TH+}}{V_- - V_{TH-}} > \frac{I_{TH+}}{I_{TH-}}$$

$$R_X = \frac{V_{TH-}(V_+) - V_{TH+}(V_-)}{I_{TH+}(V_{TH-}) - I_{TH-}(V_{TH+})} \quad (2)$$

$$R_P = \frac{V_{TH-}(V_+) - V_{TH+}(V_-)}{I_{TH+}(V_- - V_{TH-}) + I_{TH-}(V_{TH+} - V_+)} \quad (3)$$